

PCI2050

Last Update:	9/23/05
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1      Trst – CLK timing is out of specification

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## Errata #1

### Brief Description of Issue

Trst – CLK timing is out of specification.

### Detailed Description of Issue

When PCI2050B is in 66 MHz primary, 33 MHz secondary mode, the dividing DFF is in reset when primary reset is asserted, so SCLK outputs will stay low when primary reset is asserted and the 66/33 mode is selected. When primary reset is de-asserted, the design will always have 22 secondary PCI clock cycles from the removal of primary bus reset (and the secondary bus clock starting) to the removal of secondary bus reset. So to calculate that time, it is  $22 * (1/33) = 667$  ns. However, according to the PCI specification, S\_CLK should become active 100 us before S\_RST is de-asserted. So PCI2050B is out of PCI specification. The problem does not exist when PCI2050B is in 66 MHz primary, 66 MHz secondary mode or 33 MHz primary, or 33 MHz secondary mode.

### Impact to Customer & Probability of Bug Occurring in Actual Applications

PCI2050B has been used extensively in the field, and to date, no incompatibilities have been reported.

### SW or HW Workarounds Defined

After the de-assertion of the primary reset, write a '1' to bit 6 of the Bridge Control Register to initiate a secondary bus reset. Then after 100us, write a '0' to bit 6 of the Bridge Control Register to de-assert the secondary bus reset.

Add a circuit to the S\_RST# to delay the de-assertion of secondary bus reset by 100us. .

### Affected Devices

PCI2050A, PCI2050B

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